Advance Program
IEEE International SOC Conference

September 12-15, 2004
Santa Clara Hilton , Santa Clara, California

SUNDAY, SEPTEMBER 12
Workshop Tutorials

MORNING SESSIONS:

Analog, Mixed-Signal and RF Design for SOC Applications

SA1
8:00 a.m. – 11:40 a.m.
Trade-Offs in RF Analog Circuit Design for SOC Applications
S. Farahani, S. Kiaei*, N. Darbanian, M. H. Smith**, A. Hietala***, *Freescale Semiconductor, Inc,.*Arizona State University*, ***Intel Corporation*, and ****RF Micro Devices*

SoC Design Methodology in Deep Submicron Technology

SB1
8:00 a.m. – 11:40 a.m.
SoC Design Methodology: A Practical Approach
A. Jain, *Texas Instruments, USA* and A. Saha, *Texas Instruments, India*

11:50 a.m. – 1:00 p.m. – Lunch on your own

AFTERNOON SESSIONS

Analog, Mixed-Signal and RF Design for SOC Applications

SA2
1:00 p.m. – 2:50 p.m.
Substrate Coupling Noise and its Reduction through Early Design Planning in Mixed-Signal SoCs
M. Chrzanowska-Jeske and G. Blakiewicz, *Pennsylvania State University*

SA3
3:00 p.m.– 4:50 p.m.
A 243-GHz Ft and 208-GHz Fmax, 90-nm SOI CMOS SoC Technology with Low-Power Millimeter-Wave Digital and RF Circuit Capability
N. Zamdmer, J. Kim, R. Trzcinski, J. Plouchart, S. Narasimha, *IBM*

SoC Design Methodology in Deep Submicron Technology

SB2
1:00 p.m. – 2:50 p.m.
Heterogenenous Modeling of SoCs with System C using Multi-MOC Kernel of System C
H. D. Patel and S. K. Shukla, *Virginia Tech*

SB3
3:00 p.m. – 4:50 p.m.
High-Performance CMOS Circuits for Sub-90nm Design
Steven K. Hsu, *Intel Corporation*

5:00 p.m. – 6:30 p.m. – Opening Reception

MONDAY, SEPTEMBER 13

Plenary Session
8:30 a.m. – 11:00 a.m.

OPENING REMARKS:
Sung-Mo "Steve" Kang, General Conference Chair

TECHNICAL PROGRAM OVERVIEW
Dong Ha, Technical Program Chair

KEYNOTE PRESENTATION:
Beyond Voice: The Third Generation of Wireless
Paul E. Jacobs, Executive Vice President and President,
QUALCOMM Wireless & Internet Group

PLENARY PRESENTATIONS:
Reviews and Prospects of Low-voltage RAM Circuits
Kiyoo Itoh, Fellow, Hitachi, Ltd.

The Interconnect Era of ASIC/SOC Technology
James D. Meindl, Director, Microsystems Research Center and Professor, Microsystems,
Georgia Institute of Technology

CONCURRENT SESSIONS
11:10 a.m. – 11:55 a.m.

MA1: RECONFIGURABLE APPLICATIONS
Chair: Sangin Hong, *SUNY at Stony Brook*
Co-chair: Tughrul Arslan, *University of Edinburgh*

MA1.1 **Fast Parallel Soft Viterbi Decoder Mapping on a Reconfigurable DSP Platform,** Amir Kamalizad, Richard Plettner, Chengzhi Pan, Nader Bagherzadeh, UC Irvine, Irvine, CA

MA1.2 **Video Transmission through Domain Specific Reconfigurable Architectures over Short Distance Wireless Medium utilizing Bluetooth IEEE 802.15.1™ Standard,** Imran Ahmed, Tughrul Arslan, and Sami Khawam, University of Edinburgh, Edinburgh, United Kingdom

MB1: ON-CHIP TESTING OF EMBEDDED SILICON TRANSDUCERS
Chair: Paul Lee, *Eastman Kodak*

MB1.1 **(Invited) On-chip Testing of Embedded Silicon Transducers,** Salvador Mir, Benoit Charlot, Libor Rufer, and B. Courtois, TIMA Laboratory, Grenoble, France

MC1: MULTI-THRESHOLD CIRCUITS
Chair: Wei Hwang, *National Chiao Tung University*
Co-chair: Kaijian Shi, *Synopsys, Inc.*

MC1.1 **Fast Techniques for Standby Leakage Reduction in MTCMOS Circuits,** Wenxin Wang, Mohab Anis* and Shawki Areibi, University of Guelph, Ontario, Canada and *University of Waterloo, Montreal, Canada

MC1.2 **Analysis and Design of Low-Power Multi-Threshold MCML,** Hassan Hassan, Mohab Anis, Mohamed Elmasry, University of Waterloo, Waterloo, Canada

CONCURRENT SESSIONS
1:10 p.m. – 2:50 p.m.

MA2: ANALOG TO DIGITAL CONVERSION
Chair: Andrew Marshall, *Texas Instruments*
Co-chair: Hongjiang Song, *Intel Corp.*

MA2.1 **A High-Speed Power and Resolution Adaptive Flash Analog-to-Digital Converter,** Sunny Nahata, Kyusun Choi, and Jincheol Yoo*, The Pennsylvania State University, University Park, PA and *Korea Military Academy, Seoul, Korea

MA2.2 **A Background Calibration Scheme for Pipelined ADCs Including Non-linear Operational Amplifier Gain and Reference Error Correction,** Andreas Larsson and Sameer Sonkusale, Texas A&M University, College Station, TX

MA2.3 **Analog to Digital Conversion for SONET OC-192,** A. H. Ismail and M. I. Elmasry, University of Waterloo, Waterloo, ON

MA2.4 **Parallel Time Interleaved Delta Sigma Band Pass Analog to Digital Converter for SoC Applications,** Saiyu Ren, Ray Siferd and Robert Blumgold*, Wright State University Dayton, OH and *Wright Patterson AFB, OH

MB2: SYSTEM LEVEL ARCHITECTURE AND DESIGN
Chair: Ram Krishnamurthy, *Intel Corp*.

MB2.1 **Transparent SOC: On-chip Analyzing Techniques and Implementation for Embedded Processor,** Makoto Saen, Motohiro Nakagawa*, Junichi Nishimoto*, Tomoyuki Kodama, and Fumio Arakawa, Hitachi,Ltd., Tokyo, Japan and *Renesas Technology Corp., Tokyo, Japan

MB2.2 **A Circuit-Switched Network Architecture for Network-on-Chip,** Jian Liu, Li-Rong Zheng, Hannu Tenhunen, Royal Institute of Technology (KTH), Kista, Stockholm, Sweden

MB2.3 **Clock Tree Tuning using Shortest Paths Polygon,** Haydar Saaied, Dhaimin Al-Khalili*, Asim J. Al-Khalili, Concordia University, Montreal, Canada and * Royal Military College, Kingston, Canada

MB2.4 **Multilevel Routing with Jumper Insertion for Antenna Avoidance,** Tsung-Yi Ho, Yao-Wen Chang and Sao-Jie Chen, National Taiwan University, Taipei, Taiwan, ROC

MC2: DEEP-SUBMICRON DESIGN
Chair: Raguram Venkatesan, *Intel Corp.*

MC2.1 **Signal Integrity Implications of Inductor-to-Circuit Proximity,** Radu M. Secareanu, Qiang Li, Sushil Bharatan, Carl Kyono, Rainer Thoma, Mel Miller, and Olin Hartin, Motorola Inc., Tempe, AZ

MC2.2 **POMR: A Power-Optimal Maze Routing Methodology,** Ahmed Youssef, Mohab Anis and Mohamed Elmasry, University of Waterloo, Waterloo, Canada

MC2.3 **Coaxial Polymer Pillars: Ultra-Low Inductance Compliant Wafer-Level Electrical Input/Output Interconnects for Power Distribution,** Kaveh Shakeri, Muhannad S. Bakir and James D. Meindl, Georgia Institute of Technology, Atlanta, GA

MC2.4 **Leakage Aware SER Reduction Technique for UDSM Logic Circuits,** Praveen Elakkumanan, Vishwanath Anathakrishnan, Ashok Narasimhan and Ramalingam Sridhar, SUNY at Buffalo, Buffalo, NY

CONCURRENT SESSIONS
3:10 p.m. – 4:25 p.m.

MA3: RF CIRCUITS
Chair: P.R. Mukund, *Rochester Institute of Technology*
Co-chair: Andrew Marshall, *Texas Instruments*

MA3.1 **A Generic Macromodel for Coupling between Inductors and Interconnects for R.F.I.C Layouts,** Tejasvi Das, Ghanshyam Nayak and P.R. Mukund, Rochester Institute of Technology, Rochester, NY

MA3.2 **3-22GHz CMOS Distributed Single-Balanced Mixer,** Xiaohua Fan and Edgar Sánchez-Sinencio, Texas A&M University, College Station, TX

MA3.3 **Impact of Technology Scaling on RF CMOS,** Hassan Hassan, Mohab Anis, Mohamed Elmasry, University of Waterloo, Waterloo, Canada

MB3: DESIGN AND ANALYSIS TOOLS
Chair: Dong Ha, *Virginia Tech*

MB3.1 **Silencer! A Tool For Substrate Noise Coupling Analysis,** Patrick Birrer, Terri S. Fiez, and Kartikeya Mayaram, Oregon State University, Corvallis, OR

MB3.2 **Adaptive Response Surface Modeling-based Method for Analog Circuit Sizing,** Donghoon Han and Abhijit Chatterjee, Georgia Institute of Technology, Atlanta, GA

MB3.3 **Circuit Level Modeling and Simulation of Mixed-Technology Systems,** Bo Wan, Pavel V. Nikitin, and Richard Shi, University of Washington, Seattle, WA

MC3: LOW POWER SIGNAL PROCESSING
Chair: Martin Margala, *University of Rochester*
Co-chair: Hongjiang Song, *Intel Corp*.

MC3.1 **Power-Efficient Implementation of Turbo Decoder in SDR System,** B. Kang*, N. Vijaykrishnan, M.J. Irwin, and T. Theocharides, *Samsung, Korea and Pennsylvania State University, University Park, PA

MC3.2 **A Power-Aware Scalable Pipelined Booth Multiplier,** Hanho Lee, Inha University, Incheon, Korea

MC3.3 **High Throughput and Low Power FIR Filtering IP Cores,** C.H. Wang, A.T. Erdogan and T. Arslan, University of Edinburgh, Edinburgh, United Kingdom

POSTER SESSION
4:40 p.m. – 6:00 p.m.

P1: **Synthesis of SystemC Models from SDF Ptolemy Descriptions,** Brian A. Jackson and James R. Armstrong, Virginia Tech, Blacksburg, VA

P2: **A Scalable and Robust Rail-to-Rail Delay Cell for DLLs,** Håkan Bengtson and Christer Svensson, Linköping University, Linköping, Sweden

P3: **FPGA Implementation of Efficient Kalman Band-Pass Sigma-Delta Filter for Application in FM Demodulation,** Charayaphan Charoensak and Saman S. Abeysekera, Nanyang Technological University, Singapore

P4: **System-Level Design of Low-Cost FPGA Hardware for Real-Time ICA-Based Blind Source Separation,** Charayaphan Charoensak and Farook Sattar, Nanyang Technological University, Singapore

P5: **A 0.13µm 1Gb/s/channel Store-and-Forward Network on-Chip,** Filippo Mondinelli, Michele Borgatti* and Zsolt M. Kovacs Vajna, University of Brescia, Italy and *STMicroelectronics, Italy

P6: **A Memory Allocation and Assignment Method Using Multi-Way Partitioning,** Namhoon Kim and Ralph Peng, University of Southern California, Los Angeles, CA

P7: **Low-Power Driven Standard-Cell Placement Based on a Multilevel Force-Directed Algorithm,** Yu-Hsiung Huang and Mely Chen Chi, Chung Yuan Christian University, Chung Li, Taiwan

P8: **Mixed-Signal DFE for Multi-Drop, Gb/s, Memory Buses - a Feasibility Study,** Henrik Fredriksson and Christer Svensson, Linköping University, Linköping, Sweden

P9: **Bandgap yield loss due to dislocations on RFSiGe transceiver ICs: Failure analysis, design improvements and process solutions,** Ralph Oberhuber, Christoph Hechtl, Klaus Schimpf and Berthold Staufer, Texas Instruments Deutschland GmbH, Freising, Germany

P10: **A Novel Phase Detector for PAM-4 Clock Recovery in High Speed Serial Links,** Kahn-Li Lim and Zeljko Zilic, McGill University, Montreal, Canada

P11: **An Efficient Reformulation Based Architecture for Adaptive Forward Error Correction Decoding In Wireless Applications,** Yao Gang, Tughrul Arslan and Ahmet Erdogan, Edinburgh University, Edinburgh, United Kingdom

P12: **A New Level Shifter in Ultra Deep Sub-Micron for Low to Wide Range Voltage Applications,** Kyoung-Hoi Koo, Jin-Ho Seo, Myeong-Lyong Ko and Jae-Whui Kim, Samsung Electronics, Yongin City, Korea

P13: **Design of a Programmable Crypto-Processor for Multiple Crypto-Systems,** Jeemyong Lee, Wooseok Kwon, Sanghun Lee and Chanho Lee, Soongsil University, Seoul, Korea

P14: **Exploration of GFP Frame Delineation Architectures for Network Processing,** Ciaran Toal and Sakir Sezer, Queens University Belfast, Belfast, United Kingdom

P15: **Reducing Crosstalk Noise in High Speed FPGAs,** Arindam Mukherjee, University of North Carolina, Charlotte, NC

P16: **Coarse-grain Reconfigurable XPP Devices for Adaptive High-End Mobile Video Processing,** Juergen Becker and Martin Vorbach*, Universitaet Karlsruhe (TH), Karlsruhe, Germany and *PACT XPP Technologies AG, Munich, Germany

P17: **Robust Multi-Phase Clock Generation with Reduced Jitter,** Kalle Folkesson and Christer Svensson, Linköping University, Linköping, Sweden

P18: **A Low Clock Load Conditional Flip-flop,** Martin Hansson, and Atila Alvandpour, Linköping University, Linköping, Sweden

P19: **Crosstalk Induced Fault Analysis in DRAMs,** Zemo Yang and Samiha Mourad, Santa Clara University, Santa Clara, CA

P20: **A Synchronous Interface for SoCs with Multiple Clock Domains,** Visvesh Sathe, Conrad Ziesler, Marios Papaefthymiou, Suhwan Kim*, and Stephen Kosonocky**, University of

Michigan, Ann Arbor, MI, *Seoul National University, Seoul, Korea and **IBM TJ Watson Research Center, Yorktown Heights, NY

P21: **Achieving Higher Dynamic Range in Flash A/D Converters,** N. Stefanou and S. R. Sonkusale, Texas A&M University, College Station, TX

P22: **Low Energy Transmission Coding for On-Chip Serial Communications,** Kangmin Lee, Se-Joong Lee, and Hoi-Jun Yoo, Korea Advanced Institute of Science and Technology, Daejeon, Korea

P23: **Clock Tree Layout Design for Reduced Delay Uncertainty,** Dimitrios Velenis, Marios C. Papaefthymiou*, and Eby G. Friedman**, Illinois Institute of Technology, Chicago, IL, *University of Michigan, Ann Arbor, MI and **University of Rochester, Rochester, NY

BANQUET
6:00 p.m. – 8:00 p.m.
Guest Speaker: Dr. Michael Riordan, Adjunct Professor, University of California, Santa Cruz

TUESDAY, SEPTEMBER 14

CONCURRENT SESSIONS
8:40 a.m. – 10:20 a.m.

TA1: EMBEDDED PROCESSORS FOR SOC
Chair: Christopher Ryan, *Vitesse Semiconductor*
Co-chair: Arindam Mukherjee, *UNC Charlotte*

TA1.1 **A 800 MHz PowerPC SOC with PCI-X DDR266, DDRII-667, and RAID Assist,** Gerard Boudon, Alan Wall*, Joe Foster**, Barry Wolford*, and John Fakiris***, IBM Microelectronics, Corbeil-Essonnes, France, *IBM Microelectronics, Austin, TX, **Hewlett-Packard, Houston, TX, and ***Applied Micro Circuits Corp., Cary, NC

TA1.2 **An Embedded Read Only Memory Architecture with a Complementary Cell and Two Interchangeable Power/Performance Design Points,** Steven Eustis, IBM Microelectronics, Essex Junction, VT

TA1.3 **A Generic Reconfigurable Neural Network Architecture Implemented as a Network on Chip,** Theocharis Theocharides, Gregory M. Link, N. Vijaykrishnan, M. J. Irwin, and Vamsi Srikantam*, The Pennsylvania State University, University Park, PA and *Agilent Technologies

TA1.4 **Application Specific Instruction Memory Transformations for Power Efficient, Fault Resilient Embedded Processors,** Raid Ayoub, Peter Petrov* and Alex Orailoglu, University of California at San Diego, San Diego, CA and *University of Maryland, College Park, MD

TB1: HIGH PERFORMANCE SYSTEMS AND ARCHITECTURES
Chair: Thomas Buechner, *IBM Germany*
Co-chair: Sanu Mathew, *Intel Corp.*

TB1.1 **Multi-Processor SoC Integration: A Case Study on BlueGene/L,** Pascal Nsame, and Yvon Savaria*, IBM, Essex Junction, VT and *Polytechnic Montreal, Montreal, Canada

TB1.2 **Communication on a Segmented Bus Platform,** Tiberiu Seceleanu, University of Turku, Turku, Finland

TB1.3 High Speed Mixed Analog/Digital PRML Architecture for Optical Data Storage System, Maxim Konakov, Jae-Wook Lee, Junghyun Lee, Eun-Jin Ryu, Eingseob Cho, Jungeun Lee, Hyunsu Chae, Jeongwon Lee, Samsung Advanced Institute of Technology, Yongin-City, Korea

TB1.4 A High-performance Parallel Mode EBCOT Encoder Architecture Design for JPEG2000, Yun Long, Chunhui Zhang and Fadi Kurdahi, University of California, Irvine, CA

CONCURRENT SESSIONS
10:40 a.m. – 11:25 a.m.

TA2: DESIGN FOR TESTABILITY AND RELIABILITY
Chair: Ram Sridhar*, SUNY at Buffalo*
Co-chair: Ram Krishnamurthy, *Intel Corp*.

TA2.1 SRAM Word-oriented Redundancy Methodology Using Built In Self-Repair, Jihyun Lee, Young Jun Lee, Yong-Bin Kim, Northeastern University, Boston, MA

TA2.2 On-Chip Network Based Embedded Core Testing, Jong-Sun Kim, Min-Su Hwang, Seungsu Roh, Ja-Young Lee, Kangmin Lee*, Se-Joong Lee*, and Hoi-Jun Yoo*, System Integration & Intellectual Property Authoring Center (SIPAC), Deajeon, Korea and *Korea Advanced Institute of Science & Technology, Daejeon, Korea

TA2.3 An Efficient Error Masking Technique for Improving the Soft-Error Robustness of Static CMOS Circuits, Srivathsan Krishnamohan and Nihar R. Mahapatra, Michigan State University, East Lansing, MI

TB2: LOW POWER DESIGN
Chair: Arindam Mukherjee, *UNC Charlotte*

TB2.1 Low-Power On-Chip Bus Architecture Using Dynamic Relative Delays, Maged Ghoneima and Yehea Ismail, Northwestern University, Evanston, IL

TB2.2 Battery-Efficient Task Execution on Portable Reconfigurable Computing Platforms, Balasubramanian Sethuraman, Jawad Khan, and Ranga Vemuri., University of Cincinnati, Cincinnati, OH

TB2.3 A Leakage-Tolerant Low-Leakage Register File with Conditional Sleep Transistor, Amit Agarwal, Kaushik Roy and Ram Krishnamurthy*, Purdue University, West Lafayette, IN and *Intel Corp., Hillsboro, OR

12:15 p.m.
Luncheon with guest speaker:

IBM ASIC Design TAT Reduction
Dr. Jürgen Koehl (Start at 12:50 PM)
Distinguished Engineer, IBM Technology Group

CONCURRENT SESSIONS
1:40 p.m. – 3:20 p.m.

TA3: HIGH PERFORMANCE CIRCUITS AND METHODOLOGIES
Chair: Sanu Mathew, *Intel Corporation*
Co-chair: Thomas Buechner, *IBM Germany*

TA3.1 MOS Current Mode Logic: Design, Optimization, and Variability, Hassan Hassan, Mohab Anis, and Mohamed Elmasry, University of Waterloo, Waterloo, Canada

TA3.2 **A 32Kb SRAM Cache Using Current Mode Operation and Asynchronous Wave-Pipelined Decoders,** Michael Wieckowskian and Martin Margala, University of Rochester, Rochester, NY

TA3.3 **Simultaneous Bidirectional PAM-4 Link with Built-In Self-Test,** Ming-ta Hsieh and Gerald E. Sobelman, University of Minnesota, Minneapolis, MN

TA3.4 **Retiming and Clock Scheduling to Minimize Simultaneous Switching,** A. Mukherjee and R. Sankaranarayan, University of North Carolina, Charlotte, NC

TB3: NETWORK PROCESSING ARCHITECTURES AND CIRCUITS
Chair: Sakir Sezer, *Queens University Belfast*
Co-chair: Tughrul Arslan, *University of Edinburgh*

TB3.1 **(Invited) Network Processors for Access Networks(NP4AN): Trends and challenges,** Xiaoning Nie, Ulf Nordqvist, Lajos Gazsi, and Dake Liu*, Infineon Technologies, Munich, Germany and *Linkoping University, Linkoping, Sweden

TB3.2 **A WFQ Finishing Tag Computation Architecture and Implementation,** C. McKillen and S. Sezer, Queens University of Belfast, Belfast, United Kingdom

TB3.3 **An Asynchronous On-Chip Network Router with Quality-of-Service (QoS) Support,** Tomaz Felicijan and Steve Furber, The University of Manchester, Manchester, United Kingdom

CONCURRENT SESSIONS
3:40 p.m. – 4:55 p.m.

TA4: RECONFIGURABLE ARCHITECTURES
Chair: Juergen Becker, *Universitaet Karlsruhe (TH)*
Co-chair: Arindam Mukherjee, *UNC Charlotte*

TA4.1 **An Optically Differential Reconfigurable Gate Array using a 0.18μm CMOS Process,** Minoru Watanabe and Fuminori Kobayashi, Kyushu Institute of Technology, Fukuoka, Japan

TA4.2 **Rapid Energy Estimation of Computations on FPGA based Soft Processors,** Jingzhao Ou and Viktor K. Prasanna, University of Southern California, Los Angeles, CA

TA4.3 **A Virtual Channel Router for On-chip Networks,** Nikolay Kavaldjiev, Gerard J. M. Smit, Pierre G. Jansen, University of Twente, Enschede, The Netherlands

TB4: VARIOUS ISSUES OF SOC
Chair: Tughrul Arslan, *University of Edinburgh*
Co-chair: Christoher A. Ryan, *Vitesse Semiconductor*

TB4.1 **An Adaptive 4-PAM Decision-Feedback Equalizer for Chip-to-Chip Signaling,** Marcus van Ierssel, Joyce Wong and Ali Sheikholeslami, University of Toronto, Toronto, Canada

TB4.2 **Substrate Noise Optimization in Early Floorplanning for Mixed Signal SOCs,** Grzegorz Blakiewicz, Marcin Jeske and Malgorzata Chrzanowska-Jeske, Portland State University, Portland, OR

TB4.3 **A New Multi-Channel On-Chip-Network Architecture for System-On-Chips,** Sanghun Lee, Chanho Lee and Hyukjae Lee*, Soongsil University, Seoul, Korea and *Seoul National University, Seoul, Korea

ICU VENDOR FAIR AND RECEPTION
5:00 p.m. – 7:45 p.m.

WEDNESDAY, SEPTEMBER 15

CONCURRENT SESSIONS
8:40 a.m. – 10:20 a.m.

WA1: ANALOG CIRCUITS I
Chair: Hongjiang Song, *Intel Corp.*
Co-chair: Tughrul Arslan, *University of Edinburgh*

WA1.1 **Analysis and Design of Monolithic, High PSR, Linear Regulators for SoC Applications,** Vishal Gupta, Gabriel A. Rincon-Mora and Prasun Raha*, Georgia Institute of Technology, Atlanta, GA and * Texas Instruments, Inc.

WA1.2 **High-gain high-speed operational amplifier in digital 120nm CMOS,** Franz Schlögl, Horst Dietrich and Horst Zimmermann, Vienna University of Technology, Vienna, Austria

WA1.3 **A Compensation Technique for Transistor Mismatch in Current Mirrors,** Sripriya R. Bandi and P.R. Mukund, Rochester Institute of Technology, Rochester, NY

WA1.4 **A New Design for Built-In Self-Test of 5GHz Low Noise Amplifiers,** Jee-Youl Ryu and Bruce C. Kim, Arizona State University, Tempe, AZ

WB1: INTERCONNECT MODELING
Chair: Emrah Acar, *IBM*
Co-chair: Arindam Mukherjee, *UNC Charlotte*

WB1.1 **Decoupling Capacitors for Power Distribution Systems with Multiple Power Supply Voltages,** Mikhail Popovich and Eby G. Friedman, University of Rochester, Rochester, NY

WB1.2 **Low Power Repeaters Driving *RC* Interconnects with Delay and Bandwidth Constraints,** Guoqing Chen and Eby G. Friedman, University of Rochester, Rochester, NY

WB1.3 **Global Interconnect Optimization with Simultaneous Macrocell Placement and Repeater Insertion,** Yuantao Peng and Xun Liu, NC State University, Raleigh, NC

WB1.4 **Mutual Inductance Modeling for Multiple *RLC* Interconnects with Application to Shield Insertion,** Junmou Zhang and Eby G. Friedman, University of Rochester, Rochester, NY

CONCURRENT SESSIONS
10:40 a.m. – 11:55 a.m.

WA2: WIRELESS COMMUNICATION
Chair: Won Namgoong, *USC*
Co-chair: Sumer Can, *Intersil Corp*.

WA2.1 **A Novel Half-Rate Architecture for High-Speed Clock and Data Recovery,** Qiurong He and Milton Feng, The University of Illinois at Urbana-Champaign, Urbana, IL

WA2.2 **SoC Design of Remote Terminals for Wireless Telemetry System,** Wonjae Lee, Sangyun Hwang* Minho Kwon, Seongjoo Lee, and Jaeseok Kim, Yonsei University, Seoul, Korea

WA2.3 **An Improved Delay-Hopped Transmitted-Reference Ultra Wideband Architecture,** Xiaomin Chen and Sayfe Kiaei, Arizona State University, Tempe, AZ

WB2: DIGITAL SIGNAL PROCESSING
Chair: Tranh Tran, *Texas Instruments*
Co-chair: Hongjiang Song, *Intel Corp*.

WB2.1 **VLSI Design and Analysis of a Critical-band Transform Processor for Speech Recognition,** Chao Wang, Yit-Chow Tong and Yu Shao, Nanyang Technological University, Singapore

WB2.2 **An Application-Specific Processor Hard Macro for Real-time Control,** Xiaofeng Wu, Vassilios Chouliaras and Roger Goodall, Loughborough University, Loughborough, United Kingdom

WB2.3 **FPGA-Efficient Phase-to-I/Q Architecture,** Ireneusz Janiszewski, Hermann Meuth, and Bernhard Hoppe, University of Applied Sciences Darmstadt, Darmstadt, Germany

1:10 p.m. – 2:40 p.m.
PANEL DISCUSSION
EDA vs Design

CONCURRENT SESSIONS
2:50 p.m. – 4:50 p.m.

WA3: ANALOG CIRCUITS II
Chair: Sumer Can, *Intersil Corp*
Co-chair: Won Nangoong, *USC*

WA3.1 **A 3.8GHz Channel-Select Filter Using 0.18µm CMOS,** Jiandong Ge and Anh Dinh, University of Saskatchewan, Saskatoon, Canada

WA3.2 **Optimum Design and Trade-offs for a Triple-band LNA for GSM, WCDMA and GPS Applications,** Nazanin Darbanian*, Sayfe Kiaei, and Shahin Farahani*, Arizona State University, Chandler, AZ and *Freescale Semiconductors, Inc.

WB3: LOW POWER ARCHITECTURE
Chair: Hsien-Hsin S. Lee, *Georgia Institute of Technology*

WB3.1 **(Invited) Extended Dynamic Voltage Scaling for Low Power Design,** Bo Zhai, David T. Blaauw, Dennis Sylvester, and Krisztian Flautner*, University of Michigan, Ann Arbor, MI and *ARM Ltd., Cambridge, United Kingdom

WB3.2 **ChipPower : An Architecture-Level Leakage Simulator,** Yuh-Fang Tsai, Ananth Hegde Ankadi, N. Vijaykrishnan, Mary Jane Irwin, and Theo Theocharides, Penn State University, University Park, PA

WB3.3 **CoolPression -- A Hybrid Significance Compression Technique for Reducing Energy in Caches,** Mrinmoy Ghosh, Weidong Shi, and Hsien-Hsin S. Lee, Georgia Institute of Technology, Atlanta, GA